REMARKS

As a preliminary matter, applicants reassert the arguments presented in Amendment E, filed on July 2, 2010.

New claim 13 recites the same subject matter as claim 10, which was inadvertently cancelled in Amendment E. Accordingly, applicant addresses the examiner's rejection of claim 10 as it applies to new claim 13.

Go (U.S. Patent No. 6,320,566) shows, in Fig. 10, a controller IC that generates a first clock signal FD1 and a second clock signal FD2, such that second clock signal is 180° out of phase with respect to the first clock signal. A data driver IC 120 that receives the clock signals FD1 and FD2 as inputs. The data driver IC 120 also includes a latch and multiple XOR gates 160, the XOR gates divided into two groups. The first group of gates 160 receives, as inputs, the first clock signal FD1 and a video signal from a first group of output terminals of the latch, while the second group of gates 160 receives, as inputs, the second clock signal FD2 and a video signal from a second group of output terminals of the latch.

However, Go fails to disclose (or suggest) a selection signal as recited in new claim 13. While the examiner asserts that "the clock signal generator selects either the first clock signal or the second clock signal depending on if the odd or even lines are receiving the first or second latch signals," applicants could find no support for such a statement in Go. Instead, Go merely provides display data and both the first and second clock signals to the data driver IC at all times. The display data is provided to the latch in the data driver IC,

which then splits the display data among its multiple outputs. Each of the latch outputs is connected to an XOR gate, along with one of the clock signals FD1 and FD2 (see Go col. 6, line 66 – col. 7, line 5). The XOR gates in the data driver IC generate a LOW phase pulse when both inputs are the same and a HIGH phase pulse when the two inputs are different (see Go col. 7, lns. 10-13, Table 1). Thus, the clock signals serve to invert the display data while a clock provides a HIGH phase pulse, and leaves the display data signal unaffected when the clock provides a LOW pulse. However, there is no indication that any selection signal is generated.

Further, because Go fails to disclose generating a selection signal, it logically follows that the reference also fails to disclose selecting a first or second clock signal based on the selection signal and selectively latching data signals with the first or second clock signal, as recited in new claim 13. Instead, Go teaches that both clock signals are used so that output data generated by the XOR gates that receive clock signal FD1 as an input is applied to odd-numbered pixels in a data line, while output data generated by XOR gates that receive clock signal FD2 as an input is applied to even-numbered pixels in a data line (col. 7, lns. 36-43). This allows the display of Go to function using a dot inversion method. However, it is clear that Go uses both clocks simultaneously to create this effect, and does not select one of the two clocks, as recited in the present claim. For at least these reasons, applicants assert that newly added claim 13 is allowable.

For all of the above reasons, applicant requests reconsideration and allowance of the claimed invention. The examiner should contact applicant's undersigned attorney if a telephone conference would expedite prosecution.

If a Petition under 37 C.F.R. §1.136(a) for an extension of time for response is required to make the attached response timely, it is hereby petitioned under 37 C.F.R. §1.136(a) for an extension of time for response in the above-identified application for the period required to make the attached response timely. The Commissioner is hereby authorized to charge fees which may be required to this application under

Respectfully submitted,

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